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EXAMINER	
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ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,856	MEARES, LAWRENCE G.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-12 and 15-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8-12,15,17-36,38 and 39* is/are rejected.

7)☒ Claim(s) *7,16 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: non-final

Introduction

1. Title is: SYSTEM AND METHOD OF PROVIDING ADDITIONAL CIRCUIT ANALYSIS USING SIMULATION TEMPLATES
2. First named inventor is: MEARES
3. Claims 1-3, 6-12, 15-39 have been submitted, examined. Claims 1, 10 and 31 are independent claims.
4. This office action is in response to Applicant's Request for Continued Examination (RCE) received on 8/20/2004.
5. The amendments are accepted without objection.
6. Claims 1-3, 6, 8-12, 15, 17-36, 38-39 are rejected. Claims 7, 16, and 37 are objected to.

Index of Important Prior Art

7. Tucker refers to The Computer Science and Engineering Handbook, by Allen B. Tucker, Jr., CRC Press, ISBN 0-8493-2909-4, 1996, Page 862-863 sensitivity analysis, and Page 2348 simulation models.
8. Bair refers to US Patent 5,278,769.
9. Beyer refers to Handbook of Mathematical Sciences 5th Edition, by William H. Beyer, CRC Press, ISBN 0-8493-0655-8, 1978, Page 726 Mean Deviation, and Page 727 Standard Deviation, and Page 727 Root Mean Square.
10. Dorf referes to The Electrical Engineering Handbook, by Richard Dorf, 1993.
11. Chonnad refers to US Patent 6,601,024.

Definitions

12. **Optimization** is defined as "[MATH] The maximizing or minimizing of a given function possibly subject to some type of constraints. [SYS ENG] 1. Broadly, the efforts and processes of making a decision, a design, or a system as perfect, effective, or functional as possible. 2. Narrowly, the specific methodology, techniques, and procedures used to decide on the one specific solution in a defined set of possible alternatives that will best satisfy a selected criterion. Also known as system optimization." by McGraw–Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1329, 1989. Emphasis added.

13. **Simulate** is defined as " [ENG] To mimic some or all of the behavior of one system with a different, dissimilar system, particularly with computers, models, or other equipment", according to McGraw-Hill Dictionary of Scientific and Technical Terms, Fourth Edition, page 1737, 1989.
14. **Simulation** is defined as "the imitation of the operation of a real-world process or system over time. Simulation involves the generation of an artificial history of the system and the observation of that artificial history to draw inferences concerning the operating characteristics of the real system that is represented. Simulation is an indispensable problem-solving methodology for the solution of many real-world problems. Simulation is used to describe and analyze the behavior of a system, ask what-if questions about the real system, and aid in the design of real systems. Both existing and conceptual systems can be modeled with simulation." by The Handbook of Simulation, Jerry Banks, 1998, pages 3-4.

Applicant's Remarks

15. The Examiner will follow the Applicant's headings:
16. (I) INFORMATION DISCLOSURE STATEMENT. Remarks page 14, Applicant has provided all the proper information regarding item Y, and item AA of the IDS. Item AA has been considered under the redundant listing as item W, "Table of Component Failure Modes..." on the form PTO-892. Thus, the record does show that the publication has been considered by the Examiner.
17. (II) DRAFTSMAN OBJECTIONS-ABEYANCE. Remarks page 15, said objections are held in abeyance until allowable subject matter is indicated.
18. (III) OBJECTION TO THE SPECIFICATION-WITHDRAWN. Remarks page 15. The Examiner withdraws the prior objection to the term "sensitivity".
19. Applicant defines sensitivity as **"the vector calculated when a parameter value is varied from nominal minus the vector measurement when the parameter value is nominal"** at Specification page 8, lines 8-10. The Examiner interprets the Applicant's definition as implicitly equivalent to the Tucker definition.
20. Applicant further asserts that this definition is "not inconsistent" with the "rates of change" definition of sensitivity given by Tucker. See Tucker's definition at Page 862, "Sensitivity analysis refers to methods of calculating the **rates of change** of : (1) response quantities...(2)

optimum design variable values". Note that Webster defines **"rate of change"** as "a value that results from dividing the change in a function of a variable by the change in the variable..."

21. Specifically, Applicant asserts "Tucker does not mention anything about division" at Remarks page 15. However, Tucker states "rates of change", and Webster defines "rate of change" as "a value that results from **dividing** the change in a function of a variable by the change in the variable...". Emphasis added.
22. Thus, the Tucker definition, as clarified by the Webster definition, clearly implies a division or some type of normalization or fixed change. This type of division or normalization is inherent and essential for the term sensitivity.
23. Applicant's discussion of non-linearities is valid in that the calculated sensitivities of non-linear functions may vary depending upon the size of the change in the variable. This problem may be minimized by keeping the size of the change in the variable small, relative to the non-linearity of the function.
24. Also, Applicant's definition would be acceptable if the change in the parameter value was defined or fixed. For example, sensitivity relative to a one volt change in the parameter. Otherwise, different changes in the parameter value would yield different sensitivities even in a linear function.
25. DORF. Remarks page 15. Applicant's definition from Dorf page 682 states "A measure of the extent to which a given circuit performance is affected by a given component within the circuit", should be interpreted in view of Dorf page 676 "Sensitivity... a measure of the extent to which **a change in the value** of any given component affects the response of the filter..." Emphasis added. Dorf does not explicitly disclose the division or normalization, but one of ordinary skill would recognize the division or normalization as implied, and would interpret Dorf as meaning "change in the response of the filter due to a fixed or given or nominal change in the value of a given component", or interpret Dorf as meaning "divided by or normalized by a change in the value".
26. The fundamental mathematical basis for sensitivity is as an approximation for the derivative of a function. If the function is linear, then the derivative will be a constant, and the sensitivity will be constant under all conditions. However, if the function is non-linear, and

then the sensitivity at or about a given value of the variable is only an approximation of the derivative. Further, the sensitivity of a non-linear function at a given variable value may change depending upon the magnitude of the change in the variable used to calculate the sensitivity. The sensitivity will approach the derivative as the change in the variable approaches zero (assuming a well behaved non-linear function with no discontinuities). See the fundamental theorem of calculus regarding derivatives. Basically, a sensitivity is a slope based upon 2 points, the change in height divided by the change in width.

27. In conclusion, the Applicant has provided documentation (Dorf) showing that the definition of sensitivity in technical publications often omits explicit mention of division or normalization. Thus, Applicant's definition is accepted, and is interpreted as consistent with Tucker.
28. All objections to the specification are withdrawn.
29. (IV) CLAIM INTERPRETATION. Remarks page 17. Applicant asserts that the term "routine" should be interpreted as "one or more commands", citing specification page 8 and 10. This definition is consistent with the specification, and consistent with the Examiner's prior definition. The Examiner adopts Applicant's definition.
30. Remarks page 18. Applicant defines "nominal selected vector" and "nominal value for said selected vector" as meaning "a selected vector measurement in a reference simulation when the circuit parameters are at their nominal values". The Examiner accepts this definition.
31. (V) CLAIM REJECTIONS 35 USC 103. Applicant has substantially amended the claim limitations, and also added new claims. Thus, new rejections are provided below.
32. Regarding claim 1 at Remarks page 21-23, Applicant asserts that Bair does not disclose altering "circuit parameter" values per claim 1. Bair column 3 line 10 states "different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".
33. Applicant apparently asserts that the claim 1 term "circuit parameter" excludes power supply voltage and temperatures. However, the term claim 1 term "circuit parameter" is quite broad, and apparently can include power supply voltage and temperatures.
34. Regarding claim 2, note that Bair column 1 line 59 discloses "Circuit simulators, such as SPICE and its many variants, model a circuit in very great detail. All circuit elements are

modeled in an analog fashion, and transistors are very complete, taking into account many of the actual physical characteristics of the device... extremely accurate... parasitic capacitances". Thus, Bair's "actual physical characteristics of the device" also discloses the claim 1 term "circuit parameter".

35. Claim 4 and claim 5 have been cancelled.

36. Regarding claim 6, at Remarks page 25 Applicant asserts that Tucker's page 862 discussion of "sensitivity analysis" does not disclose "performing a sensitivity analysis of an electric circuit". The Examiner concedes that Tucker's discussion of sensitivity analysis does occur in the context of Chapter 36 "Computational Structural Mechanics", and not in the context of electric circuit design. However, note that Tucker is titled "The Computer Science and Engineering Handbook". Further note that the analogous properties of mechanical and electrical systems are well known to one of ordinary skill in the art of simulation. For example, electrical system voltage is analogous to mechanical system potential energy, the underlying mathematics is identical.

37. Regarding legal precedent (making automatic), the Examiner adopts Applicant's definition of "routine", and has revised the rejections accordingly. Thus, MPEP 2144.04(III) regarding *In re Venner* is no longer used in the rejections.

38. Regarding legal precedent (eliminating element), Applicant presents a detailed analysis of the facts of *Ex parte Wu*, 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989), from MPEP 2144.04(II.A). For convenience, the entire section of the MPEP 2144.04(II) is provided below:

> II. ELIMINATION OF A STEP OR AN ELEMENT AND ITS FUNCTION
> Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired
> Ex parte Wu , 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989) (Claims at issue were directed to a method for inhibiting corrosion on metal surfaces using a composition consisting of epoxy resin, petroleum sulfonate, and hydrocarbon diluent. The claims were rejected over a primary reference which disclosed an anticorrosion composition of epoxy resin, hydrocarbon diluent, and polybasic acid salts wherein said salts were taught to be beneficial when employed in a freshwater environment, in view of secondary references which clearly suggested the addition of petroleum sulfonate to corrosion inhibiting compositions. The Board affirmed the rejection, holding that it would have been obvious to omit the polybasic acid salts of the primary reference where the function attributed to such salt is not desired or required, such as in compositions for providing corrosion resistance in environments which do not encounter fresh water.). See also In re Larson, 340 F.2d 965, 144 USPQ 347 (CCPA 1965) (Omission of additional framework and

> axle which served to increase the cargo carrying capacity of prior art mobile fluid carrying unit would have been obvious if this feature was not desired.); and In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (deleting a prior art switch member and thereby eliminating its function was an obvious expedient).
> B. Omission of an Element with Retention of the Element's Function Is an Indicia of Unobviousness
> Note that the omission of an element and retention of its function is an indicia of unobviousness. In re Edge, 359 F.2d 896, 149 USPQ 556 (CCPA 1966) (Claims at issue were directed to a printed sheet having a thin layer of erasable metal bonded directly to the sheet wherein said thin layer obscured the original print until removal by erasure. The prior art disclosed a similar printed sheet which further comprised an intermediate transparent and erasure-proof protecting layer which prevented erasure of the printing when the top layer was erased. The claims were found unobvious over the prior art because the although the transparent layer of the prior art was eliminated, the function of the transparent layer was retained since appellant's metal layer could be erased without erasing the printed indicia.).

39. Applicant distinguishes the facts of Ex parte Wu from claim 1, asserting that *Ex parte Wu* is limited to methods of decreasing corrosion rate in the chemical and material science arts, and does not apply to the instant claims regarding software simulation of circuits. These assertions are not persuasive, because the underlying legal principle is that omission of an element and its function is obvious if the function of the element is not desired, and this broad legal principle is not limited to chemical and material science arts.
40. Further, Applicant does not assert that the element is eliminated while the function is retained, which would be indicia of nonobviousness per MPEP 2144.04(II.B).
41. **Regarding claim 7, Applicant is correct that Beyer does not disclose root sum squared analysis between the selected vector measurements and the nominal (or base, or reference, or golden) values for said selected vector measurements. Rather, Beyer uses the mean values as a basis for analysis, not the nominal values. Thus, claim 7 appears to contain allowable subject matter, and is merely objected to for depending from a rejected claim material.** Claims 16 and 37 are similar to claim 7.
42. The revised claim interpretations and new rejections are presented below.

Claim Interpretation

43. The claim language is interpreted in light of the specification. Limitations from the specification must not be imported into the claims, but definitions from the specification must be imported into the claims.

44. In Claim 1, the Examiner hereby interprets **"routine"** as "one or more commands". For example, "perturbing routine" is interpreted as one or more commands performing the desired "perturbing". See Applicant's remarks.
45. In Claim 1, **"netlist"** is interpreted as a list describing electrical or logical components and their connections.
46. In Claim 6, the Examiner hereby interprets **"sensitivity analysis"** according Applicant's definition: "the vector calculated when a parameter value is varied from nominal minus the vector measurement when the parameter value is nominal" at Specification page 8, lines 8-10. And the Examiner further interprets the Applicant's definition as consistent with Tucker's definition, as discussed above, and implicitly divided or normalized by the change in the parameter value.
47. In Claims 7, 8, and 9, the Examiner hereby interprets **"nominal selected vector measurement"** as a basis or reference for calculations. Note that claim 5 has been amended in such a way as to support this interpretation.

Claim Objections

48. Dependent claims 7, 16, and 37 are objected to as depending from rejected claims. These dependent claims would be allowable if rewritten in independent form and incorporating all of the limitations of the independent claims from which they depend, as well as the limitations of all intervening claims.

Claim Rejections - 35 USC § 103

49. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
50. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.

51. Claims 1-3, 6, 8-12, 15, 17-36, 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable.

52. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bair in view of Chonnad.

53. Claim 1 is an independent claim with 4 limitations, labeled by the Examiner for clarity. Note that limitation 1 has two parts.

54. [1 part 1]-**"adding a first simulation routine to said SPICE netlist** [to perform a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements]" is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".

55. [2]-**"adding a perturbing routine to said SPICE netlist for altering circuit parameter values of said circuit design in a pre-determined manner"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".

56. Note that Applicant has defined "routine" as "one or more commands". Further note that Bair discloses "several different simulated conditions of power supply... best and worst case", which implies a first case of maximum power (best), and a second case of minimum power (worst).

57. [3]-**"adding a second simulation routine to said SPICE netlist for performing simulations of said circuit design for respective altered circuit parameter values to arrive at respective selected vector measurements"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard

simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".

58. Note that Applicant has defined "routine" as "one or more commands". Further note that Bair discloses "several different simulated conditions of power supply... best and worst case", which implies a first case of maximum power (best), and a second case of minimum power (worst).

59. [4]-**"adding an analysis routine to said SPICE netlist for manipulating at least one of said selected vector measurements in accordance with said pre-determined analysis"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".

60. Bair does not expressly disclose the remaining limitation 1 part 2.

61. [1 part 2]-"[adding a first simulation routine to said SPICE netlist] **to perform a reference simulation of said SPICE netlist to arrive at nominal values for selected vector measurements"** is disclosed by Chonnad FIG 1 element 18 "REFERENCE OUTPUT VECTORS", which are also known as "golden output vectors" at column 2 line 18. In other words, a base set of input vectors is used to generate a base set of output vectors (reference output vectors, or golden output vectors, or nominal output vectors) for the base system. Any changes in the system ("parameter perturbations" in the Applicant's terminology) are evaluated by comparison of the new output vectors against the reference output vectors.

62. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad's base (or nominal, or reference, or golden) set of output vectors to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43. Starting with a base case and performing sensitivity

analysis with respect to the critical parameters is common search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.

63. Claims 2-3, 6, and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blair in view of Chonnad and MPEP § 2144.04(II)(A) Legal Precedent (eliminating element) and Tucker.
64. In claim 2, **"adding tolerances in the SPICE netlist for said circuit parameters"** is disclosed by Bair at Column 3 line 12 "determine the worst and best case delay characteristics, rise and fall times".
65. In claim 3, **"removing parameter and vector save statements in said SPICE netlist"** is disclosed by Legal Precedent (eliminating element). Specifically, MPEP § 2144.04(II)(A) states "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired". The save statements are omitted because it is not desired to save the parameters and vectors during this analysis. Removing the save statements speeds the simulation and saves memory, there are no unexpected results from this omission, so MPEP 2144.04(II)(B) does not apply.
66. Claims 4-5 are cancelled.
67. In claim 6, **"pre-determined analysis includes a sensitivity analysis involving a difference between said respective selected vector measurements and said nominal values for said selected vector measurements"** is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of : (1) response quantities...(2) optimum design variable values".
68. Claim 7 is objected to, but is not rejected.
69. In claim 8, **"extreme value analysis"** is disclosed by Bair at Column 3 line 11 "different simulated conditions...best and worst case".
70. In claim 9, **"worst case by sensitivity analysis involving a maximum of an absolute value of said difference between said respective selected vector measurements and said nominal selected vector measurements"** is disclosed by Bair at Column 3 line 5

"simulation results which will give best indication of the delay characteristics" and Column 3 line 12 "determine worst and best case".

71. MOTIVATION FOR CLAIMS 2-3, 6, and 8-9. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad and MPEP § 2144.04(II)(A) Legal Precedent (eliminating element) and Tucker to modify Blair. One of ordinary skill in the art would use Chonnad's base (or nominal, or reference, or golden) set of output vectors and to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43.
72. Further, one of ordinary skill in the art would be further motivated to use perform Tucker's sensitivity analysis with respect to the critical parameters as a search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.
73. Additionally, one of ordinary skill in the art would be motivated to use MPEP § 2144.04(II)(A) Legal Precedent (eliminating element) to remove the save statements to speed the simulation and saves memory, there are no unexpected results from this omission, so MPEP 2144.04(II)(B) does not apply.
74. Claims 10-12, 15, and 17-18 are "computer readable medium" claims with the same limitations as Claims 1-3, 6, and 8-9 above, and thus are rejected for all the same reasons.
75. Claim 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bair in view of Chonnad.
76. Claims 19-23 are "method" claims depending directly or indirectly from claim 1.
77. In claim 19, **"said circuit parameter values of said circuit design are one of resistance of a resistor, capacitance of a capacitor, and inductance of an inductor"** is implicitly disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are

standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".

78. In claim 20, **"said at least one selected vector measurement is voltage at a node of said circuit design"** is implicitly disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".
79. In claim 21, **"said at least one selected vector measurement is current along a branch of said circuit design"** is implicitly disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".
80. In claim 22, **"said at least one selected vector measurement is power dissipation in a component of said circuit design"** is implicitly disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".
81. In claim 23, **"said component of said circuit design is one of a resistor, a capacitor, and an inductor"** is implicitly disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".
82. MOTIVATION FOR CLAIMS 19-23. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad and MPEP § 2144.04(II)(A) Legal Precedent (eliminating element) and Tucker to modify Blair. One of ordinary skill in the art would use Chonnad's base (or nominal, or reference, or golden) set of output vectors and to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43.
83. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bair in view of Chonnad and Tucker.

84. Claim 24 depends from claim 1.

85. In claim 24, **"only one circuit parameter value of said circuit design is altered at a time by the perturbing routine"** is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of : (1) response quantities...(2) optimum design variable values". Note that altering a single parameter value at a time is the most common or basic use of sensitivity analysis. See Tucker's definition at Page 862, "Sensitivity analysis refers to methods of calculating the **rates of change** of : (1) response quantities...(2) optimum design variable values". Note that Webster defines **"rate of change"** as "a value that results from dividing the change in a function of a variable by the change in the variable..." Note that Webster states "change in the variable", which is singular, and implies that a single variable is changed at a time, and that sensitivity is generally with respect to change in a single variable. Sensitivity due to simultaneous changes in multiple variables is much more complex (due to non-linear interactions between the multiple variables), and is used in advanced quality control analysis, but is beyond the scope of the present discussion.

86. MOTIVATION FOR CLAIM 24. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad and Tucker to modify Blair. One of ordinary skill in the art would use Chonnad's base (or nominal, or reference, or golden) set of output vectors and to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43.

87. Further, one of ordinary skill in the art would be further motivated to use perform Tucker's sensitivity analysis with respect to the critical parameters as a search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.

88. Claims 25-30 are "computer readable medium" claims with the same limitations as claims 19-24, and are rejected for the same reasons.
89. Claims 31-36, and 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blair in view of Chonnad and Tucker.
90. Claim 31 is an independent "method" claim.
91. In claim 31, limitation (a), **"providing a SPICE netlist of a circuit design"** is disclosed by Bair at column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".
92. In claim 31, limitation (b), **"selecting a selected vector measurement of the circuit design"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times". Also see column 2 line 52 "SPICE is a "standard simulator" which has grown into a de-facto industry standard over a number of years... HSPICE", and column 4 line 24 "netlist".
93. In claim 31, limitation (d), **"altering at least one circuit parameter value of a component in the SPICE netlist in a pre-determined manner to generate at least one altered circuit parameter value"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".
94. In claim 31, limitation (e), **"simulating the SPICE netlist of the circuit design with the at least one altered circuit parameter value to determine an altered vector measurement associated with the selected vector measurement"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".
95. In claim 31, limitation (f), **"repeating steps (d) and (e) with the at least one circuit parameter value to generate a plurality of altered circuit parameter value to generate a plurality of altered circuit parameter values and to determine a plurality of altered vector measurements of the circuit design"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply

voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

96. The remaining limitations (c) and (g) are not expressly disclosed by Blair.

97. In claim 31, limitation (c), **"simulating the SPICE netlist of the circuit design using nominal circuit values to determine a nominal vector measurement associated with the selected vector measurement"** is Chonnad FIG 1 element 18 "REFERENCE OUTPUT VECTORS", which are also known as "golden output vectors" at column 2 line 18. In other words, a base set of input vectors is used to generate a base set of output vectors (reference output vectors, or golden output vectors, or nominal output vectors) for the base system. Any changes in the system ("parameter perturbations" in the Applicant's terminology) are evaluated by comparison of the new output vectors against the reference output vectors.

98. In claim 31, limitation (g), **"determining a difference between the plurality of altered vector measurements and the nominal vector measurement to generate a sensitivity in the vector measurement of the circuit design in response to alterations in the at least one circuit parameter value of the component in the SPICE netlist"** is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of : (1) response quantities...(2) optimum design variable values".

99. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad's base (or nominal, or reference, or golden) set of output vectors to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43. Starting with a base case and performing sensitivity analysis with respect to the critical parameters is common search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.

100. Further, one of ordinary skill in the art would be further motivated to use perform Tucker's sensitivity analysis with respect to the critical parameters as a search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.

101. Claims 32-39 depend directly or indirectly from claim 31.

102. In claim 32, **"a simulation template is used to perform steps (b)-(g)"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

103. In claim 33, **"the at least one circuit parameter value of the component in the SPICE netlist is altered within a tolerance of the component"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

104. In claim 34, **"the at least one circuit parameter value of a component is one of resistance of a resistor, capacitance of a capacitor, and inductance of an inductor"** is disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".

105. In claim 35, **"the vector measurement of the circuit design is one of voltage at a node, current along a branch, and power dissipation in the component"** is disclosed by Bair column 4 line 24 "netlist". Note that resistors, capacitors, and inductors are standard circuit components. Also see column 1 line 60 "circuit elements... voltages and currents".

106. In claim 36, **"only one circuit parameter value of said circuit design is altered at a time"** is disclosed by Tucker at Page 862 "Sensitivity analysis refers to methods of calculating the rates of change of : (1) response quantities...(2) optimum design variable values".

107. Claim 37 is not rejected, but is merely objected to, similar to claim 7 above.

108. In claim 38, limitation [1], **"the at least one circuit parameter value is altered to a maximum value and the SPICE netlist of the design is simulated to determine a first altered vector measurement"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

109. In claim 38, limitation [2], **"the at least one circuit parameter is altered to a minimum value and the SPICE netlist of the circuit design is simulated to determine a second altered vector measurement"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

110. In claim 38, limitation [3], **"determined a maximum of a first absolute value of the first altered vector measurement less the nominal vector measurement and a second absolute value of the second altered vector measurement less the nominal measurement to determine an extreme value analysis (EVA) for the vector measurement of the circuit design"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

111. In claim 39, limitation [1], **"determining scalar differences between the plurality of altered vector measurements and the nominal vector measurement"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

112. In claim 39, limitation [2], **"taking the absolute value of the scalar differences to generate absolute scalar differences"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

113. In claim 39, limitation [3], **"determining a worst case by sensitivity (WCS) for the selected vector measurement of the circuit design"** is disclosed by Bair at Column 3 line 10 "The circuit-level simulation is run under several different simulated conditions of power supply voltage and temperature characteristics to determine the worst and best case delay characteristics, rise and fall times".

114. MOTIVATION FOR CLAIMS 32-36, and 38-39. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Chonnad and Tucker to modify Blair. One of ordinary skill in the art would use Chonnad's base (or nominal, or reference, or golden) set of output vectors and to modify Bair in order to establish a starting point for iterative circuit modifications while optimizing the design of the circuit. Additionally, note that Bair implicitly discloses, or at least teaches towards Chonnad's base set of output vectors at Column 4 line 52 "input file preparation and ouput file analysis". One of ordinary skill in the art would have been motivated to do this "Because of the labor-intensive nature of logic/timing model generation" according to Bair at Column 3 line 43.

115. Further, one of ordinary skill in the art would be further motivated to use perform Tucker's sensitivity analysis with respect to the critical parameters as a search technique for objective criteria optimization. Sensitivity analysis supports predictions (assuming local linearity), which reduces the number of simulations required to find an optimum solution. This type of searching has some drawbacks, such as the tendency to find only a local optimum and not the global optimum, and thus is often combined with genetic algorithm methods.

Patentable material

116. At present, the Examiner believes that this application contains some potentially patentable material. Specifically, claim 7 states "a root summed square analysis involving a sum of the square of said difference between said respective selected measurements and said nominal values for said selected vector measurements". The prior art Beyer discloses "standard deviation" which is very similar but which is based upon the mean value, rather than based upon the nominal values as in claim 7. Claims 16 and 37 are similar to claim 7.

Conclusion

117. Thus, claims 7, 16, and 37 are objected to, but are not rejected.

118. Claims 1-3, 6, 8-12, 15, 17-36, 38-39 are rejected.

Communication

119. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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